

REMARKS**Objection to the Declaration**

The examiner objected to the declaration because the full name of the second inventor, R. V. Giridhar, is not provided. The patent rules (37 C.F.R. §1.1 et seq.) only require the declaration to include the inventor's name. (See 37 C.F.R. §1.41.) The rules no longer require the name to include the family name and at least one given name without abbreviation. That requirement was removed from 37 C.F.R. §1.41, when the rule was revised several years ago. (Compare the current version of 37 C.F.R. §1.41 with the previous version, copies enclosed.) Moreover, the pending application and U.S. Patent No. 6,350,651 (copy enclosed), which is derived from a related application, identify the second inventor in the same way – further evidencing that the manner in which the second inventor is identified in the pending application is proper.

For these reasons, applicants' declaration, which properly identifies the second inventor as R. V. Giridhar, is not defective. Accordingly, applicants request the examiner to withdraw the objection to the declaration.

Objection to claims 12-14

The examiner objected to claims 12-14 because the phrase "the flash cell floating gate" should be "the flash memory cell's floating gate." In response, applicants have amended claim 12 to specify "the flash memory cell's floating gate" instead of "the flash cell floating gate." Given this amendment, applicants request the examiner to withdraw this objection.

Rejection Under 35 U.S.C. §102(b)

The examiner rejected claims 9-11 and 15 under 35 U.S.C. §102(b) as being anticipated by Kiyohiko. In response, applicants amended claim 9 to clarify that applicants' flash memory comprises a passivation layer that covers the flash memory cell. Support for this amendment appears in the specification at page 6, line 3, through page 7, line 2, which describe forming an ultraviolet ("UV") opaque passivation layer by depositing a barrier layer and then a stress reduction layer. As explained in this portion of the specification, the barrier layer may comprise silicon nitride, which may be deposited using a conventional plasma enhanced chemical vapor deposition ("PECVD") process. The stress reduction layer may comprise a polyimide, which may be spun onto the silicon nitride layer. Because these PECVD and spin-on processes deposit these materials over the entire structure, the resulting passivation layer must necessarily cover the device's flash memory cells – as well as all of the other features that are integrated into the device.

not true

Kiyohiko does not describe a flash memory that anticipates the flash memory of pending claims 9-11 and 15. As the examiner recognized, Kiyohiko describes an EPROM. EPROMs and flash memories are different types of devices. EPROMs are programmable read only memories that are erased by exposing them to UV radiation. In contrast, flash memories are programmable read only memories that are erased electronically. The examiner should note that the other cited reference, Jeuch, distinguishes EPROMs from flash

memories at column 1, lines 6-11. Because Kiyohiko describes an EPROM –
not a flash memory, that reference does not anticipate claims 9-11 and 15.

Kiyohiko does not anticipate those claims for another reason. Claim 9, as amended, requires the UV opaque passivation layer to cover the flash memory cell. Because flash memories do not require UV exposure to erase them, they may remain operable even when their flash memory cells are covered with such a passivation layer. In contrast, Kiyohiko's EPROM, which requires UV exposure to erase it, must permit UV radiation to reach its memory cells. For that reason, Kiyohiko's device must include its window 11, which is formed within polyimide film 10, to enable UV radiation to reach its memory cells. Because Kiyohiko's EPROM does not (and cannot) include a passivation layer that covers its memory cells, Kiyohiko's device does not anticipate the flash memory of applicants' claims 9-11 and 15 for this additional reason.

The claimed invention relates to flash memories, not EPROMs. In addition, the claimed invention requires the passivation layer to cover the flash memory cell – a feature that Kiyohiko's EPROM lacks. For these reasons, Kiyohiko does not anticipate the flash memory of amended claim 9. Because claims 10, 11 and 15 depend upon amended claim 9, Kiyohiko does not anticipate those claims either. Accordingly, applicants request the examiner to withdraw the rejection of these claims based upon Kiyohiko allegedly anticipating them.

Rejection Under 35 U.S.C. §103(a)

The examiner rejected claims 12-14 under 35 U.S.C. §103(a) as being unpatentable over Kiyohiko in view of Jeuch. These claims depend upon amended claim 9. As explained above, amended claim 9 requires the UV opaque passivation layer to cover the flash memory cell. Neither Kiyohiko nor Jeuch describes a flash memory that includes this feature. Nor does either reference provide any teaching or suggestion that would have motivated one skilled in the art to modify any of the devices they describe by incorporating into them an UV opaque passivation layer that covers a flash memory cell.

On the contrary, Kiyohiko teaches away from including such a feature in such a device. Kiyohiko teaches to form a window through the passivation layer to enable UV radiation to reach the memory cells. Because Kiyohiko's EPROM can be erased only by exposing the memory cells to UV radiation, modifying that device such that an UV opaque passivation layer covers the memory cells would have rendered it inoperable. Because those skilled in the art would have recognized that covering the memory cells in Kiyohiko's EPROM with an UV opaque passivation layer would yield an inoperative device, it would not have been obvious to them to modify that device in that way.

Unlike Kiyohiko's EPROM, flash memories do not require UV exposure to erase them. For that reason, they may be erased even when their flash memory cells are covered with an UV opaque passivation layer. Notwithstanding that fact, conventional wisdom – prior to applicants' invention – held that even flash memories could not include an UV opaque passivation layer that covers the flash

memory cells. The reason why is because even these devices' memory cells required UV exposure to neutralize any electronic charge that had built up on the memory cells during the process for making the device. Because that UV exposure step was performed after the passivation layer was formed, it was not possible for the device to include an UV opaque passivation layer that covered the flash memory cells.

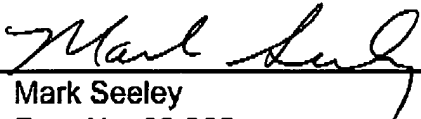
Applicants discovered that such an UV exposure step could effectively neutralize electric charge -- even when applied before forming the passivation layer, as long as that UV exposure step was performed after patterning the final metal layer. Applicants' process for forming a flash memory, which includes applying an UV exposure step prior to forming the passivation layer, is the subject of U.S. Patent No. 6,350,651, copy enclosed. Not until applicants invented that patented process was it even possible to make the flash memory of amended claim 9, which includes an UV opaque passivation layer that covers the flash memory cell. It logically follows that the claimed flash memory is patentable for essentially the same reasons that the process for making it is patentable -- as the Patent Office previously acknowledged when issuing the enclosed patent.

For the reasons set forth above, the flash memory of amended claim 9 is patentable over the combination of Kiyohiko and Jeuch. Because claims 12-14 depend upon amended claim 9, they are likewise patentable over the cited prior art. Consequently, applicants request the examiner to withdraw the rejection of these claims based on 35 U.S.C. §103(a).

The flash memories claimed in all pending claims are patentable over the cited references, either when considered alone or in combination. Accordingly, applicants respectfully request the examiner to allow pending claims 9-15, as amended, to issue.

Respectfully submitted,

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**VERSION OF AMENDED CLAIMS WITH
MARKINGS TO SHOW CHANGES MADE**

9. (Amended) A flash memory comprising:

a semiconductor substrate that includes a flash memory cell that has a floating gate;

a conductive layer formed on the substrate; and

a passivation layer formed on the conductive layer that is not transparent to ultraviolet light, the passivation layer covering the flash memory cell. } - new matter

12. (Amended) The flash memory of claim 11 wherein the flash memory cell's floating gate has a gate length that is less than about 0.5 microns.

CERTIFICATE OF TRANSMISSION
(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being transmitted by facsimile to the United States Patent and Trademark Office on September 12, 2002.

Mark Sealey
Name of Person Sending Facsimile

Mark Sealey
Signature